

What is Claimed:

- 1 1. A process for fabricating an electronic device, the process
2 comprising:
- 3 (a.) forming a first dopant blocking layer at a first temperature; and
4 (b.) forming a second dopant blocking layer at a second temperature
5 over said first dopant blocking layer.
- 1 2. A process as recited in claim 1, wherein said first temperature is
2 lower than said second temperature.
- 1 3. A process as recited in claim 1, wherein the process further
2 comprises:
3 forming a third dopant blocking layer between said first and said second
4 dopant blocking layers.
- 1 4. A process as recited in claim 1, wherein said first dopant blocking
2 layer is formed over a vertical sidewall of a mesa and over a horizontal surface of a
3 substrate; and
4 said first dopant blocking layer has a substantially uniform thickness.
- 1 5. A process as recited in claim 1, wherein said first and said second
2 blocking layers are InAlAs.
- 1 6. A process as recited in claim 3, wherein said third dopant blocking
2 layer is chosen from the group consisting essentially of InP, InGaP, InGaAs, or InGaAsP.
- 1 7. A process as recited in claim 1, wherein said first temperature lies
2 in the range of approximately 500°C to approximately 570°C.
- 1 8. A process as recited in claim 4, wherein said thickness is in the
2 range of approximately 50 nm to approximately 100 nm.
- 1 9. A process as recited in claim 1, wherein said second dopant
2 blocking layer has a vertical portion and said vertical portion has a thickness in the range
3 of approximately 30 nm to approximately 100 nm.
- 1 10. A process as recited in claim 1, wherein said first and second
2 dopant blocking layers are InGaAlAs.

1 11. A process as recited in claim 1, wherein said first dopant blocking
2 layer is disposed above a p-type layer and said second dopant blocking layer is disposed
3 below a semi-insulating layer.

1 12. A process as recited in claim 1, wherein said first dopant blocking
2 layer is disposed below a p-type layer and said second dopant blocking layer is disposed
3 above a semi-insulating layer.

1 13. A process for fabricating an optoelectronic device as recited in
2 claim 1, wherein said second temperature lies in the range of approximately 600° C to
3 approximately 650° C.

1 14. A process as recited in claim 1, wherein said first and said second
2 dopant barrier layers are formed by MOVPE.

1 15. A process as recited in claim 1, wherein said first and said second
2 dopant barrier layers are formed by MBE.

1 16. A process as recited in claim 15, wherein said first temperature lies
2 in the range of approximately 400° C to approximately 470° C.

1 17. A process as recited in claim 15, wherein said second temperature
2 lies in the range of approximately 500° C to approximately 550° C.

1 18. A process as recited in claim 14, wherein said first temperature is
2 in the range of approximately 500°C to approximately 570° C.

1 19. A process as recited in claim 14, wherein said second temperature
2 lies in the range of approximately 600 °C to approximately 650 °C.

1 20. A process for fabricating an electronic device, the process
2 comprising:

3 (a.) forming a first InAlAs layer at a first temperature; and

4 (b.) forming a second InAlAs layer at a second temperature over said first
5 InAlAs layer.

1 21. A process as recited in claim 20, wherein said first temperature is
2 lower than said second temperature.

1 22. A process as recited in claim 20, wherein the process further
2 comprises:

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3 forming a layer of undoped InP between said first and said second InAlAs
4 layers.

1 23. A process as recited in claim 20, wherein said first InAlAs layer is
2 formed over a vertical sidewall of a mesa and over a horizontal surface of a substrate; and
3 wherein said first InAlAs layer has a substantially uniform thickness.

1 24. A process as recited in claim 20, wherein said first InAlAs layer is
2 disposed above a p-type layer and said second InAlAs layer is disposed below a semi-
3 insulating layer.

1 25. A process a recited in claim 20, wherein said first InAlAs layer is
2 disposed below a p-type layer and said second InAlAs layer is disposed above a semi-
3 insulating layer.

1 26. A process for fabricating an electronic device as recited in claim
2 20, wherein said second temperature lies in the range of approximately 600 °C to
3 approximately 650 °C.

1 27. A process as recited in claim 20, wherein said first temperature lies
2 in the range of approximately 500 °C to approximately 570 °C.

1 28. A process as recited in claim 20, wherein said first and said second
2 dopant blocking layers are formed by MOVPE.

1 29. A process as recited in claim 20, wherein said first temperature lies
2 in the range of approximately 400 °C to approximately 470 °C.

1 30. A process as recited in claim 20, wherein said second temperature
2 lies in the range of approximately 500° C to approximately 550° C.

1 31. A process as recited in claim 20 wherein said first and said second
2 dopant blocking layers are formed by MBE.

1 32. An electronic device, comprising:
2 a multilayer dopant barrier disposed between a first doped layer and a
3 second doped layer, said multilayer dopant barrier further comprising:
4 a first dopant blocking layer disposed adjacent said first doped layer; and
5 a second dopant blocking layer disposed adjacent said second doped layer.

1 33. An electronic device as recited in claim 32, wherein said first
2 doped layer is in a mesa, and said second doped layer disposed on at least one side
3 of said mesa.

1 34. An electronic device as recited in claim 33, wherein said first
2 dopant blocking layer has a vertical portion adjacent a vertical sidewall of said
3 mesa and a horizontal portion above a substrate.

1 35. An electronic device as recited in claim 32, wherein said first
2 dopant blocking layer substantially prevents dopants from diffusing out of said
3 first doped layer.

1 36. An electronic device as recited in claim 32, wherein said second
2 dopant blocking layer substantially blocks dopants from diffusing out of said
3 second doped layer.

1 37. An electronic device as recited in claim 32, wherein said first
2 dopant blocking layer is InAlAs.

1 38. An electronic device as recited in claim 32, wherein said second
2 dopant blocking layer is InAlAs.

1 39. An electronic device as recited in claim 34, wherein said vertical
2 portion and said horizontal portion have a substantially identical thickness.

1 40. An electronic device as recited in claim 32, wherein said first
2 dopant blocking layer has a resistivity in the range of approximately $10^6 \Omega\text{-cm}$ to
3 approximately $10^9 \Omega\text{-cm}$.

1 41. An electronic device as recited in claim 32, wherein said second
2 dopant blocking layer has a resistivity in the range of approximately $10^4 \Omega\text{-cm}$ to $10^5 \Omega\text{-cm}$.
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1 42. An electronic device as recited in claim 32, wherein said first
2 doped layer is p-doped InP and said second doped layer is InP(Fe).

1 43. An electronic device as recited in claim 32, wherein said first
2 dopant blocking layer substantially blocks Zn dopants and said second dopant blocking
3 layer substantially blocks iron dopants.

1 44. An electronic device as recited in claim 32, wherein the electronic
2 device is chosen from the group consisting essentially of light emitting and light detecting
3 optoelectronic devices.

1 54. An electronic device as recited in claim 48, wherein said multi-
2 layer dopant barrier further comprises:

3 a third dopant blocking layer disposed between said first and said second
4 dopant blocking layers.

1 55. An electronic device as recited in claim 54, wherein said third
2 dopant blocking layer is chosen from the group consisting essentially of InP,
3 InGaP, InGaAs and InGaAsP.

1 56. An electronic device as recited in claim 48, wherein said first
2 doped layer is p-type and said second doped layer is semi-insulating.

1 57. An electronic device as recited in claim 48, wherein said first and
2 said second dopant blocking layers are InAlGaAs.

1 58. An electronic device as recited in claim 48, the electronic device is
2 chosen from the group consisting essentially of light emitting and light detecting
3 optoelectronic devices.

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